Restriction Requirement

It is asserted in the Office Action that the Applicants' specification identifies embodiments of the invention claimed in claims 21-40 as being directed to an invention that is independent or distinct from embodiments claimed in the Application as filed because "Applicants' original claim 10 and their canceled claims [1-9 and 11-20] were all directed to the alternative invention without machine specific registers." It was further asserted that "Because the inventions are distinct for the reasons given above and the search required for claims 21-40 is not required for claim 10, restriction for examination purposes as indicated is proper." Since claims 21-40 are not directed toward a distinctly different invention, the Applicants respectfully traverse the restriction for the following reasons.

It is respectfully noted that the Application reads as follows:

> In an example embodiment, **the firmware code 210 implements microcode operations using registers which are specific to a particular machine or to a particular model of a machine. The registers are referred to herein as "Machine Specific Registers."** The machine specific registers function as an interface between the firmware 206 and the processor 204. ... In the example embodiment shown in FIG. 2A, processor 204 includes a plurality of machine specific registers (MSRs) 208. In one embodiment, **one or more of the MSRs 208 are associated with one or more functional units of the processor** 204. For example, an MSR bank may be associated with an external bus unit, while another MSR bank might be associated with the processor's cache. ... The programmed code is executed by a processor (block 504) and the **one or more registers associated with a logic unit on the processor are updated or read** in response to the execution of the programmed code (block 506). In one embodiment, one or more of the instructions in the programmed code cause the processor to move a value from one of the processor's general purpose registers to a machine specific register (MSR). **The instruction updates one or more of the bits stored in the MSR. In the example embodiment shown in FIG. 4, the CRAB bus transfers data to the MSR register to be updated. In an alternate embodiment, an instruction in the programmed code reads an MSR by moving a value in the MSR to a general purpose register**. (Application, pg. 4, line 29 - pg. 5, line 8 and pg. 7, lines 7-27.)

It is also respectfully noted that original claims 5, 6, 7, 11, 15, and 18 read as follows:

> 5. The computer system of claim 1 wherein the processor further comprises **a plurality of registers associated with one or more functional units of the processor.**

6. The computer system of claim 5 wherein **the instructions implement microcode functions by updating one or more of the plurality of registers.**

7. The computer system of claim 5 wherein **the instructions implement microcode functions by reading one or more of the plurality of registers.**

11. The method of claim 9 wherein the **one or more functions are controlled by updating one or more registers associated with a logic unit** on the processor in response to executing the programmed code

15. A method of using firmware as microcode, the method comprising:
storing programmed code in firmware external to a processor;
executing, by the processor, the programmed code;
updating **one or more registers associated with a logic unit** on the processor in response to the executing of the programmed code; and
controlling one or more functions of the logic unit on the processor based on a value stored in the one or more registers.

18. A processor comprising:
a plurality of logic units; and
one or more registers associated with each one of the plurality of logic units, the one or more registers to trigger processor hardware logic functions when one of the registers is updated in response to an external microcode instruction.

Finally, it is respectfully noted that, in addition to these recited claims, original claims 8, 16, and 19 also address the use of a register associated with a functional unit of the microprocessor, defined in the Application as a "machine specific register." Thus, a distinct and specific error in the restriction requirement arises because the term "machine specific register" has been defined as a synonym for registers associated with processor functional units. The registers associated with processor functional units, listed several times as elements in original claims 1-20, are re-listed in synonymous form as machine specific registers in claims 21-40. Thus, the embodiments claimed in claims 21-40, listing machine specific registers, are not distinctly different inventions from the embodiments claimed in claims 1-20, listing registers associated with processor functional units. Any search made which included such associated registers would also include machine specific registers, since they are the same thing. Therefore, Applicants make the

provisional election of claim 10, with traverse, to preserve their right to petition from the requirement under 37 C.F.R. § 1.144 and M.P.E.P. § 818.03(c), and respectfully request reconsideration and withdrawal of the restriction requirement as noted in M.P.E.P. § 821.01.

Rejections Under 35 U.S.C.§102

Claim 10 was rejected under 35 U.S.C.§102(b) as being clearly anticipated by Demers et al. (WO 94/12929, hereinafter "Demers"). Since Demers does not teach each and every element claimed by the Applicants, this rejection is respectfully traversed.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). In this case, Demers does not disclose "storing programmed code on a computer readable medium *external* to a processor; executing, by the processor, the programmed code; and controlling one or more functions of the processor in response to executing the programmed code, wherein the one or more functions are controlled by updating at least one machine specific register associated with a logic unit of the processor and by directly triggering hardware on the processor in response to executing the programmed code."

The Applicant's representative has carefully read pg. 8, line 25 - pg. 9, line 3 of Demers, as suggested in the Office Action. It is respectfully noted that, while the DMA 214 unit of Demers is "used for fetching microcode from a main memory, or the like (not shown)", an intermediate caching process is required to obtain the microcode prior to execution, such that the code is stored both in the main memory and the on-chip microcode RAM cache. Demers, pg. 7, lines 24-29. Cache miss logic is specifically mentioned, since "the cache miss logic in control logic block 216 freezes the datapath and the microsequencer" when the data is not found in the cache. See Demers, pg. 6, lines 18-24. Thus, Demers does not describe or teach "storing programmed code on a computer readable medium *external* to a processor; executing, by the processor, the programmed code; and controlling one or more functions of the processor in response to executing the programmed code, wherein the one or more functions are controlled by updating at least one machine specific register associated with a logic unit of the processor and

by directly triggering hardware on the processor in response to executing the programmed code," as claimed by the Applicants.

The Office Action also asserts that "it is inherent in Demers that the microcode of Demers controls one or more functions of the processor by directly triggering hardware on the processor." It is respectfully noted that this assertion is incorrect because, as observed in the application:

> In an example embodiment, the external microcode 222 implements microcode operations by controlling hardware logic on the processor 224 without the use of the registers shown in FIG. 2A. In an alternate embodiment, **the external microcode 222 implements microcode operations using the registers shown in FIG. 2A as an interface to the processor hardware logic**. In still another embodiment, the external microcode 222 implements microcode operations by a combination of using the registers shown in FIG. 2A and by directly triggering the processor hardware logic." (Application, pg. , lines -)

Thus, the Office Action has not established a *prima facie* case of inherency because, as recited in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art," citing Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). It is respectfully noted that this basis has not been provided, since the Application states that *microcode operations can be implemented using machine specific registers*, in addition to, or as an alternative to, directly triggering the processor hardware logic (also note that the combination of these options is claimed in amended claim 10).

Therefore, since Demers fails to describe a situation wherein the microcode is stored external to the processor (it is actually stored in an on-processor cache, since anything within Demers' system 200 is on-chip (see Demers, pg. 5, line29-34)), as claimed by the Applicants in claims 10, and since it is not inherent that microcode controls processor functions by directly triggering hardware on the processor, the Applicants respectfully request reconsideration and withdrawal of the rejection under § 102.

CONCLUSION

Applicants respectfully submit that claims 10 and 21-40 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney, Mark Muller, at (210) 308-5677, or the undersigned, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

HOWARD CHIN ET AL.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 15 day of October, 2002.

Jane E. Brockschink
Name

Signature